Low Phase-Noise PHEMT-Based MMIC VCOs for LMDS Applications

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Abstract: **This paper presents Pseudomorphic High Electron-Mobility Transistor based K-band voltage-controlled oscillators, which have exhibited low phase-noise properties in conjunction with output powers greater than previously reported. An appropriate nonlinear design methodology based on the optimization of transistor's load cycles was applied. A tuning range over 14% bandwidth (22.4-25.8 GHz) for the first one, and 12% bandwidth (27.8-31.5 GHz) for the second one, were obtained. Constant output power of 6 dBm and 10 dBm respectively were measured over the tuning range. Markedly low phase noise level of -89 dBc/Hz at 100 kHz offset from the carrier (24.4 GHz), and -78 dBc/Hz at 100 kHz offset from the carrier (30 GHz) were achieved. To our knowledge, these are one of the best characteristics reported for K-band solid state VCOs.**

I. INTRODUCTION

Several technologies have matured in the last few years, which work to make Local-Multipoint-Distribution-System (LMDS) applications even more feasible. Gallium Arsenide integrated circuits, digital signal processors, video compression techniques and advanced modulation systems have all made significant improvements in cost and performance. These factors have combined to create a need for a technology that has access to large bandwidth and can be deployed for low up-front costs. The modulation schemes used in digital microwave radios, for achieving high data-transmission rates up to 155 Mbytes/sec, must balance the effects of phase noise from local oscillators to meet the specifications in terms of bit error rates (BER)[1]. Therefore, these communication systems require stable, compact, local oscillator sources, to translate base-band signals to microwave frequencies.

Monolithically integrated high electron mobility transistors (HEMTs) offer a number of application benefits, including high operating frequencies, low HF noise, high reliability, and compact size. These attributes are making HEMTs the active devices of choice in many microwave and millimeterwave applications. A comparative study of the phase-noise contribution of HEMT and HBT based oscillators demonstrated that a lower up-conversion factor can be achieved with HEMTs rather than with HBTs [2-4].

Using Pseudomorphic HEMT technology, we have developed two fully monolithic K-band VCOs which have a high tuning sensitivity needed for the frequency modulation and phase locked sources in communication systems. The fabricated circuits exhibit excellent phase noise data of -89 dBc/Hz @100kHz at 24.4 GHz and -78 dBc/Hz @100 kHz at 30 GHz. An appropriate nonlinear approach was used in the VCO's design [3]. This methodology is mainly based on the optimization of the intrinsic load cycles, which provides the best insight on the active device large signal behavior. The first successful pass of these VCO designs indicates the importance of a rigorous design methodology. This paper describes the design approach, the main features of the used technology, and the monolithic circuit performances.

II. CIRCUIT DESIGN & FABRICATION

The schematic diagrams of the VCOs are based on a 0.2um Pseudomorphic-HEMT under series feedback configuration, which is realized by means of a capacitance on the source (Fig.1a and 1.b).

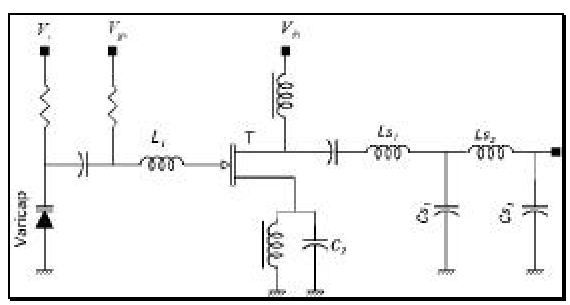

Fig.1a- 24GHz VCO Schematic

A tuning varactor diode has been introduced in the circuit connected to the gate side of the transistor, which contributes to change the equivalent inductance and results in the variation of oscillation frequency. The frequency tuning range depends on the maximum available varactor capacitance ratio. For the second VCO, a buffer amplifier was added to increase the output power level (Fig.1b).

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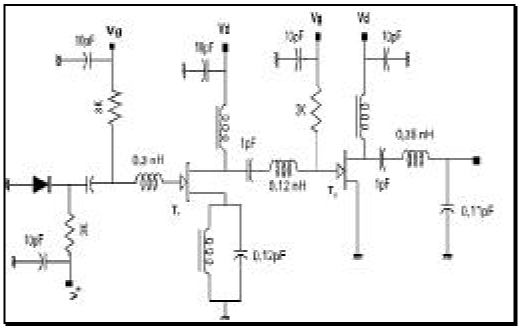

Fig.1b- 30GHz VCO Schematic.

Generally, a small signal analysis is used to derive initial element values of the circuit. A nonlinear analysis, usually harmonic balance (HB), is then performed to optimize passive elements in order to get the desired performances (frequency, power and harmonics). However, the HB oscillator analysis has a disadvantage, which is the excessive computation time due to the numerous parameters to be optimized.

Therefore, to overcome the problem, we adopted a nonlinear design optimization procedure, which consists of:

- The first step in the circuit design, classical small signal analysis is used to get the initial values of the feedback elements featuring a negative resistance at the drain terminal of the active HEMT over the desired oscillation frequency range.

- In the second step, the oscillator is transformed into a reflection amplifier and the optimization of the intrinsic load cycle allows getting optimum values of the passive feedback elements: gate inductance, and source capacitance, for each varactor control voltage.

- The final values are chosen among the optimum in order to have a near ideal load cycle over the tuning voltage. The optimum load cycle should have a minimum area (minimum reactive power), non-distorted, and featuring the largest Ids and Vds swings (Fig.2). For the final values of the capacitance and inductance, the voltage over current ratios are used to synthesize the output load in the final step.

The oscillator circuit was designed using the PML large signal models of HEMTs and varactor diodes, and was simulated with HP-MDS software.

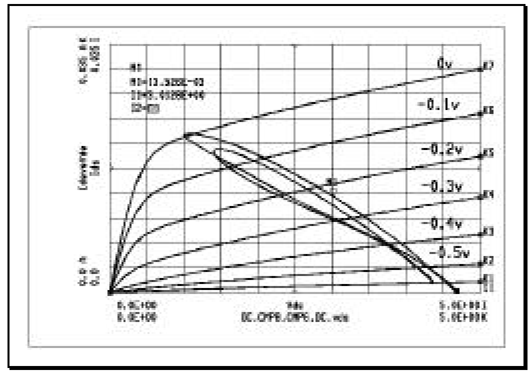

Fig.2- Dynamic Load Cycles

The circuits are fabricated using 0.2um gate length pseudomorphic HEMT GaAlAs/GaInAs/GaAs technology from Philips Microwave Limeil Foundry. The employed device with a finger width of 4x30um has a unit current gain frequency (f_t) of 62 GHz, and a minimum noise figure of 0.9 dB at 12 GHz with an associated gain of 11.5 dB. The technology further includes via-holes, epitaxial resistors and MIM capacitors. The substrate height is 100um. The varactor has an interdigitated finger structure, with length fixed to 3um, and width to 8x30um. The varactor capacitance value varies from 0.76 pF to 0.18 pF by changing the bias voltage from 0 to 1.4 V. Figure 3 shows circuit layouts. The chip sizes are 1.5 x 2 mm^2 and 3 x 2 mm^2.

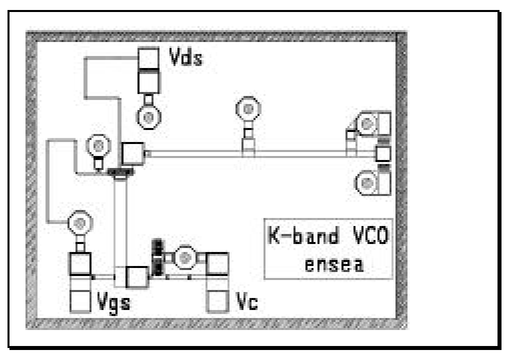

Fig.3a- 24GHz VCO Layout.

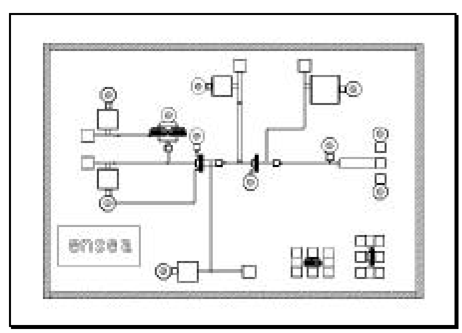

Fig.3b- 30GHz VCO Layout.

III. MEASURED MMIC PERFORMANCE

The RF performances of the VCOs were measured in a low insertion loss microstrip test fixture. Figure 4, displays the variation of the oscillation frequency as function of the varactor voltage. The results show very good agreement with the design simulations. The first oscillator is tunable over a range of 3.4 GHz and high tuning sensitivity of about 4.5GHz/V was achieved. The output power is nearly constant over the control voltage range and is about 6dBm.

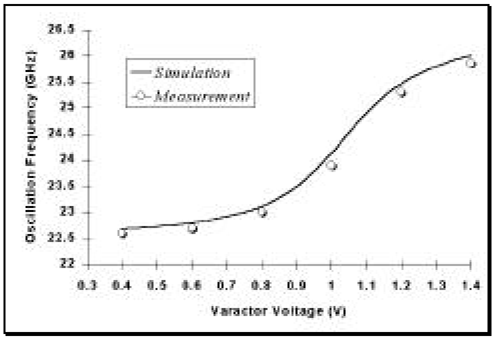

Fig.4a- Oscillation Frequency vs Varactor Voltage for Oscillator #1

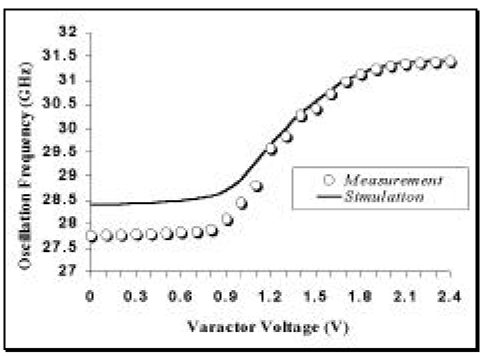

Fig 4b. Oscillation Frequency vs Varactor Voltage for Oscillator #2

The frequency pushing characteristics for drain and gate voltage are resumed in Table-1. The oscillation frequency decreases with Vgs and increases with Vds. This can be explained by the bias dependence of the HEMT equivalent circuit elements. The decrease of f_{osc} with Vgs is mainly caused by the increase of C_{gs}. However, the increase of oscillation power with Vds which is greater than the knee voltage, is related to the ratio increase of g_m/g_{ds}.

In figure 5, we have superposed two spectra of the 30 GHz oscillator, to show the tuning bandwidth.

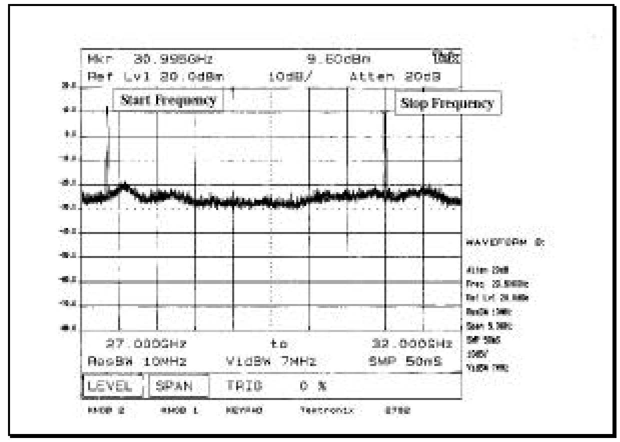

Fig.5- 30GHz oscillator's tuning bandwidth shown on a spectrum analyzer.

To investigate the oscillator phase noise performances, the single sideband frequency modulation noise, normalized to 1 Hz bandwidth, was measured for off carrier frequencies up to 100 kHz. Two phase noise measurement techniques where used. The first one based on the injection locking technique [5], and the second one based on a down-convertion using a 4-40 GHz double balanced mixer, and measured with an HP89441 Vector Spectrum Analyzer [6].

The measured phase noise Lf is less than -80 dBc/Hz @ 100 kHz over the tuning range for the 24GHz VCO. The slope of Lf curves is -30 dB/decade. The results show that the phase noise is due to the upconversion of ideal 1/f noise. Lowest phase noise of -89 dBc/Hz @ 100 kHz is observed at 24.4 GHz. For the 30GHz VCO, we measured -78 dBc/Hz @100 kHz.

To check the validity of the phase noise measurements, the transistor low-frequency noise was characterized. Baseband noise measurements on PHEMT devices featuring 4x30μm gate width and 0.2μm gate length have been carried out from 10Hz to 100KHz to determine the bias dependent low frequency noise spectra. The measured low frequency noise associated to the drain current showed fundamental $f^{-\alpha}$ noise with α =1.1 and two generation-recombinition (g-r) noise components. Each g-r noise process (Lorentzian spectrum) is related to a particular trap or defect characterized by a discret energy level E_a and a time constant τ.

Low frequency noise contribution to the oscillator phase noise was evaluated using the pushing analysis, which is based on the Kurokawa approach [7-8]. The phase noise £(f_m) model is given by :

$$£(f_m) = \frac{1}{2}\left[\frac{e_n(f_m)}{f_m}\left(\frac{\partial f_0}{\partial V_{gs}}\right)\right]^2$$

where $\partial f_o/\partial V_{gs}$ is the sensitivity of the carrier frequency with respect to the gate bias (pushing factor); $e_n(f_m)$ is the input noise voltage source featuring a spectral density $S_v(f_m) = S_i(f_m)/g_m^2$ where $S_i(f_m)$ is the drain noise current spectra and g_m is the transconductance at baseband frequency f_m.

The LF gate current noise source contribution is negligible. Basically at 10 KHz, this noise has usually been observed to be less than $Si_g(f)=10^{-24}$ A^2/Hz. We have calculated the phase noise using the measured gate pushing factor at oscillation frequency of 24.4 and 25.2 GHz. The calculated data results in £(100KHz)= -86 and -82 dBc/Hz respectively compared to the measured £(100KHz)= -89 and -83 dBc/Hz. Also, we calculated phase noise level of -82 dBc/Hz @ 100kHz at carrier frequencies 22.4 and measured -80 dBc/Hz.

We concluded that the calculated phase noise using a pushing type analysis provides a satisfactorily agreement with the measured results at different transistor bias operating points and different varactor voltages.

IV. CONCLUSION

Monolithic Pseudomorphic-HEMT VCOs have been realized using nonlinear design and optimization procedure. The measured data, which agree well with the design simulations, show a tuning bandwidth of more than 3 GHz with a constant output power of 6dBm and 10 dBm with an integrated buffer amplifier. A markedly low phase noise level of -89 dBc/Hz @ 100 kHz was measured at the frequency of 24.4 GHz and -78 dBc/Hz @100 kHz at 30 GHz.

Performance	**VCO#1 (22.4-25.8 GHz)**	**VCO#2 (27.8-31.5 GHz)**
Output Power	6 dBm	10 dBm
Tuning Bandwidth	3.4 GHz (14%)	3.7 GHz (12%)
Tuning Sensitivity	4.5GHz/V	2.7GHz/V
Lowest Phase Noise @ 100 kHz	-89dBc/Hz	-78dBc/Hz
DC Power Consumption	54 mW	96 mW
Efficiency	7.5 %	10.4 %
Freq. pushing drain bias	153 MHz/V	---
Power pushing drain bias	1.87 mW/V	---
Freq. pushing gate bias	300 MHz/V	---

Table 1. Performance of the VCOs.

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